Remarks

Claims 17-33 are pending in the application, with 17, 24, 28, 32, and 33 being the independent claims. Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

In paragraph 2 of the Office Action, claims 17-20, 24, and 25 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,317,820 to Shiell et al. (hereinafter "Shiell"). Applicant respectfully traverses this rejection. Independent claim 17 recites:

> A system to process very long instruction words (VLIWs), the system comprising:
>
> *a decode unit to decode an instruction of a VLIW received during an instruction fetch*, wherein all instructions of the VLIW have the same predetermined instruction bit length; and
>
> first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;
>
> wherein the decode unit is *operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination.*

In paragraph 10 of the Office Action, Examiner relies on col. 3, lines 60-67 of Shiell to allegedly show that Shiell teaches an instruction of a VLIW. Applicant notes that in Shiell "instructions are grouped into blocks of 8 as a single VLIW," which is referred to as an Instruction Packet. (Shiell, col. 3, lines 64-67).

Examiner relies on col. 2, lines 52-56 to allegedly show that an instruction of the VLIW can define a single operation or two independent operations. In support of this position, Examiner states, "The VLIW instructions can change the processor from the

first mode (the execution of a single operation), or the second mode (the execution of two independent operations)."

However, upon closer inspection, the "two independent operations" to which the Examiner refers are each merely "a half packet of instructions (1/2 of a VLIW eight instruction packet)." (Shiell, col. 5, lines 1-2). Thus, each of the "two independent operations" is merely a group of four instructions of the VLIW. Nothing in the cited material even suggests that *an instruction of the VLIW* can define a single operation or two independent operations. For example, Shiell does not suggest that any of the four instructions included in a half packet "independent operation" can define a single operation or two independent operations.

Examiner relies on col. 2, lines 23-56 to allegedly teach an instruction identifying whether an instruction defines a single operation or two independent operations. However, the cited material merely shows that the data processor is selectively operable in either a first or second mode. In the second mode, the data processor can process two half packets of instructions of the VLIW simultaneously. Nothing in the cited material teaches or suggests a decode unit that is *operable to determine whether an instruction* (of the VLIW) *defines a single operation or two independent operations...*, as set forth in independent claim 17.

Independent claim 24 also distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, and further in view of its own features. Furthermore, claims 18-23, which depend from claim 17, and claims 25-27, which depend from claim 24, are also patentable over Shiell for at least these reasons, and further in view of their own features. Therefore, Applicant respectfully requests that the § 102 rejections be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

In paragraph 5 of the Office Action, claims 21-23, 26, 27, and 32 were rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of U.S. Patent No. 5,761,470 to Yoshida (hereinafter "Yoshida"). Applicant respectfully traverses this rejection. Independent claim 32 recites:

> A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, the method comprising:
>
> fetching the VLIW from a program memory;
>
> *decoding each instruction of the VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine*:
>
> a) *whether the instruction defines a single operation or two independent operations*, and
>
> b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

Independent claim 32 distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, and further in view of its own features. More specifically, Shiell and/or Yoshida, alone or in combination, fail to teach or suggest *decoding each instruction of the VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine whether the instruction defines a single operation or two independent operations.*

In paragraph 12 of the Office Action, Examiner concedes that Shiell fails to teach decoding that includes reading the identification bit (at at least one predetermined bit location in the instruction) of each instruction to determine whether the instruction defines a single operation or two independent operations. Examiner relies on Figure 25 and elements 505 and 506 of Yoshida to allegedly show the missing teachings. However, Figure 25 of Yoshida merely shows a VLIW format in which one or two 1-bit

format fields are used and one VLIW includes one or two instructions. The confusion appears to be a matter of semantics.

Yoshida explains in the Background of the Invention section:

> The present invention relates to a data processor for performing a plurality of operations in parallel at a high efficiency by executing a so-called VLIW ... type instruction which specifies a plurality of operations by one instruction. (Yoshida, col. 1, lines 9-15).
>
> [T]he VLIW technique is a parallel operation technique in which one instruction consists of a plurality of parallel executable operations which are detected and encoded by a compiler at compiling time. ... the *conventional VLIW type data processor* guarantees that instructions have the same length and all of a plurality of operations which are described within one instruction can be executed in parallel.... (Yoshida, col. 1, lines 45-48) (emphasis added).

The Background to the Invention section of the present patent application provides:

> ... a number of instructions are retrieved from memory in each instruction fetch, each instruction fetch having a certain bit length and each individual instruction (slot) having a certain bit length (so-called VLIW instructions).

The instructions and operations described by Yoshida correspond to the VLIWs and instructions, respectively, described in the present patent application. In conventional VLIW operations, VLIWs (i.e. "instructions" as described by Yoshida) are retrieved from memory in each instruction fetch. Each VLIW has a first bit length, and each individual instruction has a second bit length. Although Yoshida states that *instructions* (i.e. "operations" as described by Yoshida) can be executed in parallel, nothing in Yoshida suggests a decode unit that is *operable to determine whether an instruction of the instruction sequence defines a single operation* (as described in the present patent application) *or two independent operations*, as set forth in independent claim 32.

Applicant asserts that Shiell and Yoshida, alone or in combination, fail to teach each and every feature of independent claim 32. For at least the reasons set forth above, reconsideration and withdrawal of the rejection of independent claim 32 is respectfully requested.

Claims 21-23, 26, and 27 are also patentable over Shiell and Yoshida, alone or in combination, for reasons similar to those set forth above with respect to independent claim 32, and further in view of their own features.

In paragraph 6 of the Office Action, claim 28 was rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of U.S. Patent No. 6,697,774 to Panesar (hereinafter "Panesar"). Applicant respectfully traverses this rejection. Independent claim 28 recites:

> An article comprising a medium for storing commands to enable a processor-based system to:
>
> process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, wherein *the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations*;
>
> when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel, wherein the two independent operations are executed simultaneously; and
>
> when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation.

Independent claim 28 distinguishes over Shiell for reasons similar to those set forth above with respect to independent claim 17, and further in view of its own features. Furthermore, Applicant asserts that Panesar does not supply the teachings missing from Shiell. Thus, Applicant asserts that independent claim 28 is patentable over Shiell and Panesar, alone or in combination, for reasons similar to those set forth above with respect

to independent claim 17, and further in view of its own features. Therefore, Applicant respectfully requests that the rejection of independent claim 28 be reconsidered and withdrawn.

In paragraph 7 of the Office Action, claims 29-31 and 33 were rejected under 35 U.S.C. § 103(a) as being obvious over Shiell in view of Yoshida and Panesar. Applicant respectfully traverses this rejection. Independent claim 33 recites:

> An article comprising a medium for storing commands to enable a processor-based system to:
>
> process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, wherein *the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine:*
>
> a) *whether the instruction defines a single operation or two independent operations*, and
>
> b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

Independent claim 33 distinguishes over Shiell, Yoshida, and Panesar for reasons similar to those set forth above with respect to independent claims 17, 28, and 32, and further in view of its own features. Therefore, reconsideration and withdrawal of the rejection of independent claim 33 is respectfully requested

Claims 29-31 are also patentable over Shiell, Yoshida, and Panesar, alone or in combination, for at least these reasons, and further in view of their own features.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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